Instruction Manual

Tektronix

TMS 105 386SX Microprocessor Support 070-9808-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning

The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:



WARNING. Warning statements identify conditions or practices that could result in injury or loss of life.



CAUTION. Caution statements identify conditions or practices that could result in damage to this product or other property.

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:



WARNING High Voltage



Protective Ground (Earth) Terminal



CAUTION Refer to Manual



Double Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 105 386SX microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS 105 386SX support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase "information on basic operations" refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- In the information on basic operations, the term XXX or P54C used in field selections and file names must be replaced with 386SXA. This is the name of the microprocessor in field selections and file names you must use to operate the 386SX support.
- The term system under test (SUT) refers to the microprocessor-based system from which data will be acquired.

- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.
- The term module refers to a 102/136-channel or a 96-channel module.
- 386SXA refers to all supported variations of the 386SX and 80387 microprocessors unless otherwise noted.
- A tilde (~) a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Support ment product, call toll free in North America:

1-800-TEK-WIDE (1-800-835-9433 ext. 2400)

6:00 a.m. – 5:00 p.m. Pacific time

Or, contact us by e-mail: tm_app_supp@tek.com

For product support outside of North America, contact your

local Tektronix distributor or sales office.

Service Contact your local Tektronix distributor or sales office. Or, visit

Support our web site for a listing of worldwide service locations.

http://www.tek.com

For other In North America:

information 1-800-TEK-WIDE (1-800-835-9433)

An operator will direct your call.

To write us Tektronix, Inc.

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Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics and tasks:

- A description of the TMS 105 microprocessor support package
- Logic analyzer software compatibility
- Your system under test requirements
- Support restrictions
- How to configure the probe adapter
- How to connect to the system under test (SUT)

Support Description

The TMS 105 microprocessor support package disassembles data from systems that are based on the Intel or AMD 386SX microprocessor. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel module or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 105 microprocessor support.

Table 1–1 shows the microprocessors and packages from which the TMS 105 support can acquire and disassemble data.

Table 1–1: Supported microprocessors

Name	Package
Intel/Amd 386SX	PQFP
Amd A386SXL	PQFP
Intel 80387	PQFP

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the following manuals:

- The 386SX *Microprocessor User's Manual*, Intel, 1994
- The 386SX Programmer's Reference Manual, Intel, 1994
- The 16/32-Bit Embedded Processors Manual, Intel, Inc.
- The 387SX Hardware Reference Manual, Intel, Inc.
- The *A386SX Microprocessor User's Manual*, AMD, Corp.

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the 386SXA support, the Tektronix logic analyzer must be equipped with either a 102/136-channel module, or a 96-channel module at a minimum. The module must be equipped with enough probes to acquire channel and clock data from signals in your 386SX-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other 386SX support requirements and restrictions.

System Clock Rate. The TMS 105 support can acquire data from the 386SX microprocessor at speeds of up to 25 MHz¹.

Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.

Configuring the Probe Adapter

The probe adapter does not require any configuration.

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. The probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

PQFP Probe Adapter

To connect the logic analyzer to a SUT using a PQFP probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off the logic analyzer.



CAUTION. Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all the above only in a static-free environment.

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

- 2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
- **3.** Place the probe adapter onto the antistatic shipping foam to support the probe as shown Figure 1–1. This prevents the circuit board from flexing.
- **4.** Connect the channel and clock probes to the probe adapter as shown in Figure 1–1. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

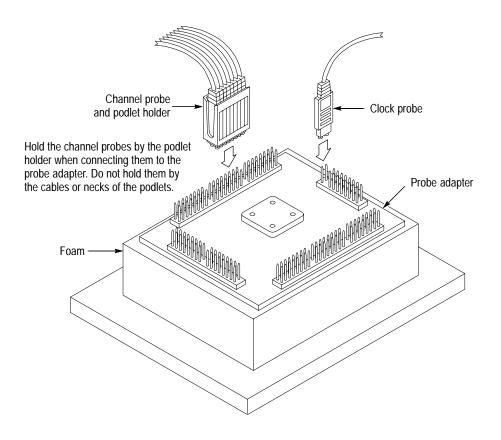


Figure 1–1: Connecting probes to a PQFP probe adapter



CAUTION. This JEDEC PQFP (Plastic Quad Flat Pack) probe adapter has been equipped with a clip that has been designed for tight tolerances.

The clip supports only Plastic Quad Flat Pack devices that conform to the JEDEC M0-069 October 1990 specification. Attaching the clip to a device that does not conform to this JEDEC standard can easily damage the clip's connection pins and/or the microprocessor, causing the probe adapter to malfunction.

Please contact your IC manufacturer to verify that the microprocessor you are targeting conforms to the JEDEC specification.

For best performance and long probe life, exercise extreme care when connecting the probe to the microprocessor.

5. Line up the pin 1 indicator on the microprocessor with the pin 1 indicator on the target head of the circuit board.



CAUTION. Failure to correctly place the probe adapter onto the microprocessor might permanently damage all electrical components when power is applied.

Center the clip on the microprocessor and apply an equal downward force on all four sides of the clip, slightly rocking the probe adapter in a clockwise circle.

Do not apply leverage to the probe adapter when installing or removing it.

6. Place the probe adapter onto the SUT as shown in Figure 1–2.

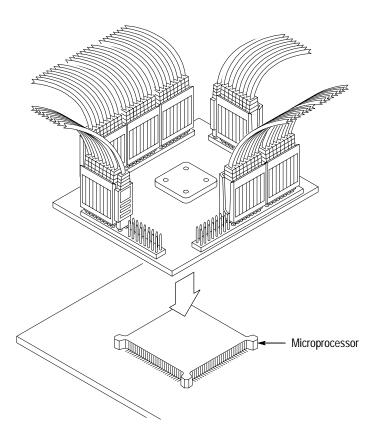


Figure 1-2: Placing a PQFP probe adapter onto the SUT



CAUTION. The probe adapter board might slip off or slip to one side of the microprocessor because of the extra weight of the probes. This can damage the microprocessor and the SUT. To prevent this from occurring, stabilize the probe adapter by placing a non-conductive object (such as foam) between the probe adapter and the SUT.

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to 386SX signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.



CAUTION. Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.

Always wear a grounding wrist strap or similar device while handling the microprocessor.

- 2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.
- **3.** Use Table 1–2 to connect the channel probes to 386SX signal pins on the test clip or in the SUT.

Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Table 1–2: 386SX signal connections for channel probes

Section:channel	386SX signal	Section:channel	386SX signal
A2:7	A23	A3:7	PEREQ*
A2:6	A22	A3:6	ERROR~*
A2:5	A21	A3:5	BUSY~*
A2:4	A20	A3:4	Not connected
A2:3	A19	A3:3	LOCK~*
A2:2	A18	A3:2	W/R~*
A2:1	A17	A3:1	D/C~*
A2:0	A16	A3:0	M/IO~*
A1:7	A15	D1:7	D15
A1:6	A14	D1:6	D14
A1:5	A13	D1:5	D13
A1:4	A12	D1:4	D12
A1:3	A11	D1:3	D11
A1:2	A10	D1:2	D10

Table 1-2: 386SX signal connections for channel probes (cont.)

Section:channel	386SX signal	Section:channel	386SX signal
A1:1	A9	D1:1	D9
A1:0	A8	D1:0	D8
A0:7	A7	D0:7	D7
A0:6	A6	D0:6	D6
A0:5	A5	D0:5	D5
A0:4	A4	D0:4	D4
A0:3	A3	D0:3	D3
A0:2	A2	D0:2	D2
A0:1	A1	D0:1	D1
A0:0	A0	D0:0	D0
C3:7	INTR_L*†	C2:7	INTR†
C3:6	Not connected	C2:6	BHE~*
C3:5	Not connected	C2:5	CLK*§
C3:4	NA_L~*†	C2:4	RESET_L*
C3:3	NMI_L*†	C2:3	NMI†
C3:2	NA~*†	C2:2	ADS~
C3:1	PIPE_D*‡	C2:1	READY~†
C3:0	HOLD*	C2:0	HLDA*†

^{*} Signal not required for disassembly.

[†] Signal not required for disassembly.

Denotes signal derived on the probe adapter.

[§] CLK2 divided by two.

Table 1–3 shows the clock probes and the 386SX signal to which they must connect for disassembly to be correct.

Table 1–3: 386SX signal connections for clock probes

Section:channel	386SX signal
CK:3	PIPE_D
CK:2	CLK
CK:1	NA_L~
CK:0	RESET_L

^{*} Denotes signals latched on the probe adapter.

[†] Signal not required for disassembly.

^{4.} Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the 386SX microprocessor in your SUT and attach the clip.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 105 386SX support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the 386SX support are Address, Data, Control, Intr (Interrupt), Copr (Coprocessor), and Misc (Miscellaneous). If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–4.

Clocking Options

The TMS 105 support offers a microprocessor-specific clocking mode for the 386SX microprocessor. This clocking mode is the default selection whenever you load the 386SXA support.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking option for the TMS 105 support is DMA Cycles. A DMA cycle is defined as the cycle in which the 386SX microprocessor gives up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included.

Symbols

The TMS 105 support supplies one symbol table file. The 386SXA_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file 386SXA_Ctrl, the Control channel group symbol table.

Table 2-1: Control group symbol table definitions

	Control group value	
Symbol	RESET_L LOCK~ BHE~ M/IO~ HLDA D/C~ READY~ W/R~	Meaning
LOCKED_RD	0 X 0 0 0 1 1 0	Non-opcode fetch locked memory read
LOCKED_WR	0 X 0 0 0 1 1 1	Any locked memory write
FETCH	0 X 0 0 X 1 0 0	Memory code read (Opcode Fetch)
MEM_READ	0 X 0 0 X 1 1 0	Non-opcode fetch memory read cycle
MEM_WRITE	0 X 0 0 X 1 1 1	Any memory write
I/O_READ	0 X 0 0 X 0 1 0	Read from an I/O port
I/O_WRITE	0 X 0 0 X 0 1 1	Write to an I/O port
MEM_RD/WR	0 X 0 0 X 1 1 X	Non-opcode fetch memory read or write
I/O_RD/WR	0 X 0 0 X 0 1 X	Read from or write to an I/O port
READ	0 X 0 0 X X 1 0	Any memory or I/O read cycle, except Opcode Fetch or Interrupt Acknowledge
WRITE	0 X 0 0 X X 1 1	Any memory or I/O write cycle
INT ACK	0 X 0 0 X 0 0 0	Responding to Interrupt

Table 2–1: Control group symbol table definitions (cont.)

	Control group value	
	RESET_L LOCK~ BHE~ M/IO~	
Symbol	HLDA D/C~ READY~ W/R	Meaning
HALT/SHUT	0 X 0 0 X 1 0 1	HALT: Address=2; SHUTDOWN: Address=0
LOCKED	0 X 0 0 0 X X X	Inseparable back-to-back cycles
RESERVED*	0 X 0 0 X 0 0 1	Reserved
DMA	0 X 1 X X X X X	Bus released to an Alternate Bus Master
HIGH_XFER	0 0 X X X X X X	Transfer on D15–D8
RESET	1 X X X X X X X	Latched RESET signal asserted

^{*} Symbols used only for triggering; they are not displayed.

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics and tasks:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- Changing the way data is displayed
- Changing disassembled cycles with the mark cycles function

Acquiring Data

Once you load the 386SXA support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to Changing How Data is Displayed on page 2–8.

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 shows these special characters and strings, and gives a definition of what they represent.

Table 2–2: Meaning of special characters in the display

Character or string displayed	Meaning
≫ or m	The instruction was manually marked as a program fetch
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks indicates the width of the data that is unavailable. Each two asterisks represent one byte.
#	Indicates an immediate value
t	Indicates the number shown is in decimal, such as #12t
(16) or (32)	Indicates that the fetch is from a 16- or 32-bit code segment size and disassembled accordingly
* ILLEGAL INSTRUCTION *	Decoded as an illegal instruction

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–3 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2-3: Cycle type definitions

Cycle type	Definition	
(CO I/O RD)	A cycle reading data from an I/O port in the coprocessor	
(CO I/O WR)	A cycle writing data to an I/O port in the coprocessor	
(DMA CYCLE)	A direct memory access cycle	
(EXTENSION)	A read cycle of either an extension long word or a word of an instruction	
(FLUSH)	Instruction flushed from the pipeline	
(HALT)	Address = 2 (Address bit 1 = 1)	
(INT ACK)	An interrupt acknowledge cycle	
(INVALID CYCLE)	An illegal cycle; an unrecognized combination of control group values	
(I/O READ)	A cycle reading data from an I/O port	
(I/O WRITE)	A cycle writing data to an I/O port	
(LOCKED MEM READ)	Any locked cycle during which data is read from memory except: opcode fetch, extension, or interrupt acknowledge	
(LOCKED MEM WRITE)	Any locked cycle during which data is written to memory	
(MEM READ)	Any cycle during which data is read from memory except: opcode fetch, extension, or interrupt acknowledge	

Table 2–3: Cycle type definitions (cont.)

Cycle type	Definition
(MEM WRITE)	Any cycle during which data is written to memory
(RESERVED)	Any cycle during which the control group bit pattern indicates reserved
(RESET)	Latched reset signal asserted
(SHUTDOWN)	Shutdown Cycle; Address = 0

Computed cycle types.

Figure 2–1 shows an example of the Hardware display.

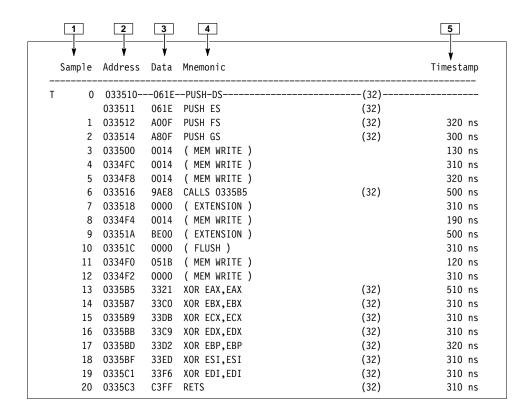


Figure 2–1: Hardware display format

- **1 Sample Column.** Lists the memory locations for the acquired data.
- **2 Address Group.** Lists data from channels connected to the 386SX Address bus.
- **3 Data Group.** Lists data from channels connected to the 386SX Data bus.

- 4 Mnemonic Column. Lists the disassembled instructions and cycle types.
- **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the 386SX microprocessor are as follows:

BOUND	JB/JNAE/JC	JNB/JAE/JNC	JNS
CALL	JBE/JNA	JNBE/JA	JO
DIV	JCXZ/JECXZ	JNE/JNZ	JP/JPE
IDIV	JE/JZ	JNL/JGE	JS
INT	JL/JNGE	JNLE/JG	LOOP
INTO	JLE/JNG	JNP/JPO	LOOPNZ/LOOPNE
IRET	JMP	JNO	LOOPZ/LOOPE
RET			

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the 386SX microprocessor are as follows:

BOUND	DIV	INT	IRET
CALL	IDIV	INTO	RET

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the 386SX support to do the following tasks:

■ Change how data is displayed across all display formats

- Change the interpretation of disassembled cycles
- Display exception vectors

There are no optional fields for this support package. Refer to the information on basic operations for descriptions of common fields.

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

- Specify the default code segment size.
- Choose an interrupt table.
- Specify the size of the interrupt table.
- Specify the starting address of the interrupt table.

The 386SX support has four additional fields: Code Segment Size, Interrupt Table, Interrupt Table Address, and Interrupt Table Size. These fields appear in the area indicated in the information on basic operations.

Code Segment Size. You can select the default code size: 32-bit or 16-bit. The default code size is 16 bit.

Interrupt Table. You can specify if the interrupt table is Real, Virtual, or Protected. (Selecting Virtual is equivalent to selecting Protected.) The default is Real.

Interrupt Table Address. You can specify the starting address of the interrupt table in hexadecimal. The default starting address is 0x00000000.

Interrupt Table Size. You can specify the size of the interrupt table in hexadecimal. The default size is 0x400.

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Extension (a subsequent word of an instruction)
- Flush (an opcode or extension that is fetched but not executed)
- Anything (any valid opcode, extension or flush)

Mark selections are as follows:

Any	01	PCODE	
OPCODE	Aı	ny	
Ext	Ex	xt	
Flush	Flush		
16-bit	Default	Segment	Size
32-bit	Default	Segment	Size

Undo marks on this cycle

You can also use the Mark Opcode function to specify the default segment size mode (16-bit or 32-bit) for the cycle. The segment size selection changes the cycle the cursor is on and the remaining cycles to the end of memory or to the next mark.

Information on basic operations contains more details on marking cycles.

Displaying Exception Vectors

The disassembler can display exception vectors. You can select to display the interrupt vectors for Real, Virtual, or Protected modes in the Interrupt Table field. (Selecting Virtual is equivalent to selecting Protected.)

You can relocate the table by entering the starting address in the Interrupt Table Address field. The Interrupt Table Address field provides the disassembler with the offset address; enter an eight-digit hexadecimal value corresponding to the offset of the base address of the exception table. The Interrupt Table Size field lets you specify a three-digit hexadecimal size for the table.

You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

Table 2–4 lists the 386SX exception vectors for the Real Addressing mode.

Table 2–4: Exception vec	tors for Real <i>A</i>	laaressing mode
--------------------------	------------------------	-----------------

Exception number	Location in IV* table (in hexadecimal)	Displayed exception name
0	0000	DIVIDE ERROR
1	0004	DEBUG EXCEPTIONS
2	0008	NMI INTERRUPT
3	000C	BREAKPOINT INTERRUPT
4	0010	INTO DETECTED OVERFLOW
5	0014	BOUND RANGE EXCEEDED
6	0018	INVALID OPCODE
7	001C	COPROCESSOR NOT AVAILABLE

Table 2–4: Exception vectors for Real Addressing mode (cont.)

Exception number	Location in IV* table (in hexadecimal)	Displayed exception name
8	0020	DOUBLE FAULT
9-11	0024-002C	RESERVED
12	0030	STACK EXCEPTION
13	0034	SEGMENT OVERRUN
14-15	0038-003C	RESERVED
16	0040	COPROCESSOR ERROR
17-31	0044-007C	RESERVED
32-255	0080-03FC	USER DEFINED

^{*} IV means interrupt vector.

Table 2–5 lists the exception vectors for the Protected Addressing mode.

Table 2–5: Exception vectors for Protected Addressing mode

Exception number	Location in IDT* (in hexadecimal)	Displayed exception name
0	0000	DIVIDE ERROR
1	0008	DEBUG EXCEPTIONS
2	0010	NMI INTERRUPT
3	0018	BREAKPOINT INTERRUPT
4	0020	INTO DETECTED OVERFLOW
5	0028	BOUND RANGE EXCEEDED
6	0030	INVALID OPCODE
7	0038	DEVICE NOT AVAILABLE
8	0040	DOUBLE FAULT
9	0048	RESERVED
10	0050	INVALID TSS
11	0058	SEGMENT NOT PRESENT
12	0060	STACK EXCEPTION
13	0068	GENERAL PROTECTION
14	0070	PAGE FAULT
15	0078	RESERVED
16	0080	COPROCESSOR MODE
17-31	0090-00F8	RESERVED
32-255	0100-07F8	USER DEFINED

^{*} IDT means interrupt descriptor table.

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your 386SX microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires 386SX signals
- List of other accessible microprocessor signals and extra probe channels

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a 386SX microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the SUT.

The probe adapter accommodates the Intel 386SX microprocessor in a 100-pin PQFP package.

Configuration

The probe adapter does not require any configuration.

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–1 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–1, for the 102/136-channel module, one podlet load is 20 k Ω in parallel with 2 pF. For the 96-channel module, one podlet load is 100 k Ω in parallel with 10 pF.

Table 3-1: Electrical specifications

Characteristics	Requirements	
SUT DC power requirements		
Voltage	4.75-5.25 VDC	
Current	I max (calculated) I typ (measured)	590 mA 395 mA
SUT clock rate	Max. 25 MHz	
Minimum setup time required		
All signals	4 ns	
Minimum hold time required		
NA~	5.5 ns	
All other signals	4 ns	
	Specification	
Measured typical SUT signal loading	AC load	DC load
Address, Data, BLE~	5 pF + 1 podlet	1 podlet
NMI, INTR, NA~	14 pF + 1 podlet	16R8–5 in parallel with 1 podlet
CLK2	10 pF	16R8–5 clock
HLDA, ADS~, READY~	9 pF + 1 podlet	1 podlet in parallel with 22V10-10
RESET	18 pF	16R8-5 + 22V10-10
All other signals	5 pF + 1 podlet	1 podlet

Table 3–2 shows the environmental specifications.

Table 3–2: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	-55° C to +75° C (-67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

^{*} Designed to meet Tektronix standard 062-2847-00 class 5.

Table 3-3 shows the certifications and compliances that apply to the probe adapter.

Table 3-3: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.

[†] Not to exceed 386SX microprocessor thermal considerations. Forced air cooling might be required across the CPU.

Figure 3–1 shows the dimensions of the probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter.

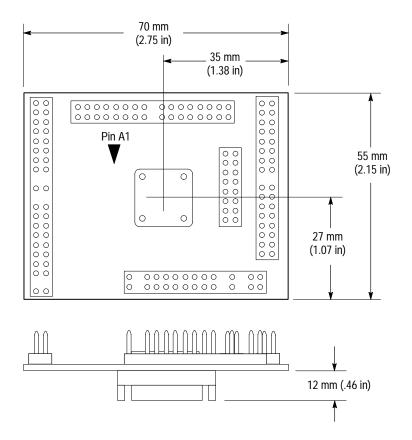


Figure 3–1: Dimensions of the probe adapter

Channel Assignments

Channel assignments shown in Table 3–4 through Table 3–10 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.

Table 3–4 shows the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-4: Address group channel assignments

Bit order	Section:channel	386SX signal name
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	А9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

Table 3–5 shows the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-5: Data group channel assignments

Bit order	Section:channel	386SX signal name
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 3–6 shows the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3-6: Control group channel assignments

Bit order	Section:channel	386SX signal name
7	C2:4	RESET_L*
6	C2:6	BHE~*
5	C2:0	HLDA* †
4	C2:1	READY~†

Table 3-6: Control group channel assignments (cont.)

Bit order	Section:channel	386SX signal name
3	A3:3	LOCK~*
2	A3:0	M/IO~*
1	A3:1	D/C~*
0	A3:2	W/R~*

^{*} Denotes signals used for disassembly.

Table 3–7 shows the probe section and channel assignments for the Intr group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–7: Intr group channel assignments

Bit order	Section:channel	386SX signal name
3	C3:3	NMI_L* †
2	C3:7	INTR_L* †
1	C2:3	NMI†
0	C2:7	INTR†

^{*} Denotes signals latched on the probe adapter.

Table 3–7 shows the probe section and channel assignments for the Copr group and the microprocessor signal to which each channel connects. By default, this channel group is displayed not visible.

Table 3-8: Copr group channel assignments

Bit order	Section:channel	386SX signal name
2	A3:5	BUSY~*
1	A3:6	ERROR~*
0	A3:7	PEREQ*

^{*} Signal not required for disassembly.

[†] Denotes signals used for micro clocking.

[†] Signal not required for disassembly.

Table 3–9 shows the probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3-9: Misc group channel assignments

Bit order	Section:channel	386SX signal name
5	C3:0	HOLD*
4	C3:4	NA_L~* †
3	C3:2	NA~* †
2	C2:2	ADS~
1	C3:1	PIPE_D* ‡
0	C2:5	CLK* §

^{*} Signal not required for disassembly.

Table 3–10 shows the probe section and channel assignments for the clock probes (not part of any group) and the 386SX signal to which each channel connects.

Table 3-10: Clock channel assignments

Section:channel	386SX signal name
CK:3	PIPE_D
CK:2	CLK
CK:1	NA_L~
CK:0	RESET_L

[†] Denotes signal latched on the probe adapter.

Denotes signal derived on the probe adapter.

[§] CLK2 divided by two.

How Data is Acquired

This part of this chapter explains how the module acquires 386SX signals using the TMS 105 software and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra probe channels available for you to use for additional connections.

Custom Clocking

A special clocking program is loaded to the module every time you load the 386SXA support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the 386SX bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

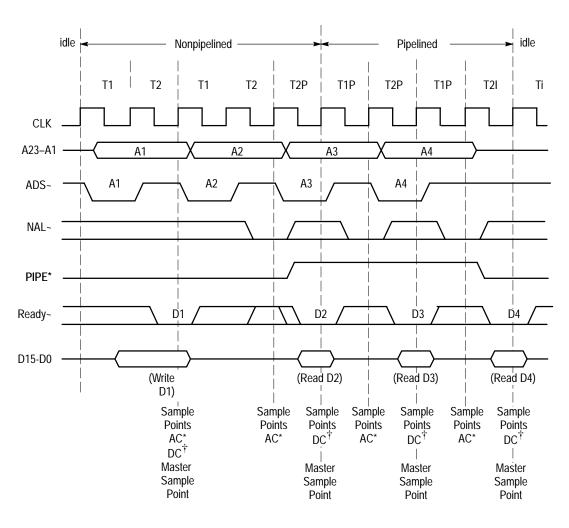


Figure 3–2 shows the sample points and the master sample point.

Figure 3–2: 386SX bus timing (pipelined and nonpipelined)

^{*} Signals sampled where AC appears are NAL~, NA~, BHE~, RESET_L, ADS~, HLDA, A23–A1, A0/BLE~, PEREQ, ERROR~, BUSY~, and FLT~.

^{*} Signals sampled where DC appears are INTR_L, NMI_L, PIPE_D, INTR, CLK, NMI, READY~, LOCK~, W/R~, D/C~, M /IO~, and D15–D0.

Clocking Options

The clocking algorithm for the 386SX support has two variations: DMA Cycles Excluded and DMA Cycles Included.

A DMA cycle is defined as any bus cycle initiated under the control of an alternate bus master. It does not need to be a DMA controller, such as an 82380. It can be another microprocessor; it need only follow the basic bus protocol of the 386SX, requiring only the CLK, NA~, ADS~, READY~, and HLDA signals. It may support bus pipelining. DMA cycles are identified by the assertion of the HLDA.

To display DMA cycles, they must appear at the 386SX socket where they can be coupled to the probe adapter. To ensure they do so, you must enable and set system buffering to route the address, data, and control bus signals to the 386SX. This buffering configuration may require modification of the system under test.

The DMA Cycles field has two options:

Excluded

Whenever HLDA is high, DMA cycles do not log or store data. Normal logging and storage resumes when HLDA returns low. Bus cycles driven by the 386SX microprocessor will be logged in.

■ Included

When HLDA is low, all bus cycles are logged in, including DMA cycles, provided system under test follows the 386SX bus transfer protocol and that its SUT bus buffer is configured (as described above) to provide DMA cycles at the 386SX socket.

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so that you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–4. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals On the Probe Adapter

All 386SX microprocessor signals are accessible on the probe adapter.

Extra Channels

Table 3–11 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Table 3-11: Extra module sections and channels

Module	Section: channels
102-channels	C3:6, C3:5, C1:7-0, C0:7-0, D3:7-0, D2:7-0, Qual:1, Qual:0
136-channels	C3:6, C3:5, C1:7-0, C0:7-0, D3:7-0, D2:7-0, E3:7-0, E2:7-0, E1:7-0, E0:7-0, Qual:3-0
96-channels	C3:6, C3:5, C1:7-0, C0:7-0, D3:7-0, D2:7-0

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This section contains a circuit description of the probe adapter.

Probe Adapter Circuit Description

The TMS 105 probe adapter accommodates the 386SX microprocessor in a 100-pin PQFP package.

The probe adapter board consists of three PALs. The first PAL, a 16R8–5, is used to divide the clock signal in half and synchronize the output with RESET. When RESET is active the output is held high.

The second PAL, another 16R8–5, is programmed to behave as a D flip-flop. It is used to latch the NMI, INTR, and NA~ signals.

The third PAL, a 22V10–10 is used to determine if the SUT is in pipelined mode. This PAL generates a PIPE_D output which remains high during a pipelined bus transaction. Since the user may press the Start key in the middle of a pipelined bus transaction, and the module has no history of what happened before the start key was pressed, this PAL allows the module to determine when to start logging signals.

The 22V10–10 also latches the RESET signal when it is active, and it remains latched until the first clock after the RESET goes inactive.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 105 386SX microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

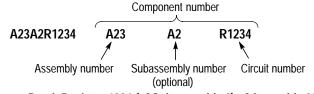
Parts list column descriptions

Column	Column name	Description	
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the <i>Diagrams</i> section, and on the mechanical exploded views in the <i>Replaceable Mechanical Parts</i> list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table).	
		The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts).	
		Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.	
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.	
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.	
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.	
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.	
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.	

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK0875	MATSUO ELECTRONICS INC	831 S DOUBLAS ST	EL SEGUNDO CA 92641
TK2058	TDK CORPORATION OF AMERICA	1600 FEEHANVILLE DRIVE	MOUNT PROSPECT, IL 60056
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769-2963
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077-0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A1	671–2441–00			CIRCUIT BD ASSY:386SX,PQFP100 SOLDERED,PROBE ADAPTER;	80009	6712441XX
A1C100	283-5003-00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	TK2058	C3216X7R1H103K-
A1C110	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A1C120	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A1C122	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A1C145	283-5003-00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	TK2058	C3216X7R1H103K-
A1C215	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A1C230	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A1C320	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A1C325	283-5003-00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	TK2058	C3216X7R1H103K-
A1C330	283-5004-00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K-
A1C340	290-5005-00			CAP,FXD,TANT:;47UF,10%,10V,5.8MM X 4.6MM	TK0875	267M-1002-476-K
A1C350	283-5003-00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	TK2058	C3216X7R1H103K-
A1J100				CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A1J120				CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A1J240				CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A1J250				CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A1J330				CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A1J345				CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A1P230				CLIP,ELEC:ASSEMBLY,PQFP10 (SEE RMPL)		
A1U100	160-8837-00			IC,DIGITAL:STTL,PLD;PAL,16R8,5NS,210MA,CLOCK-DIV	80009	160-8837-00
A1U200	160-8855-00			IC,DIGITAL:STTL,PLD;PAL,16R8,5NS,210MA,LATCH	80009	160-8855-00
A1U300	160-8838-01			IC,DIGITAL:PLD;OTP,22V10,10NS,71MHZ,180MA	80009	160-8838-00

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 105 386SX microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description	
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.	
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.	
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.	
5	Qty	This indicates the quantity of parts used.	
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook I for further item name identification.	
7	Mfr. code	This indicates the code of the actual manufacturer of the part.	
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.	

Abbreviations Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts Chassis-mounted parts and cable assemblies are located at the end of the

Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK2548	XEROX BUSINESS SERVICES DIV OF XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON OR 97077
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769-2963
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077-0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no.	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–1	131–5267–00			2	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (J100,J120,J240,J250,J330,J345)	53387	2480-6122-TB
-2	671–2441–00			1	CIRCUIT BD ASSY:386SX,PQFP100 SOLDERED,PROBE ADAPTER;	80009	671244100
					STANDARD ACCESSORIES		
	070-9808-00			1	MANUAL,TECH:INSTRUCTION,386SX,DISSASEMBLER, TMS 105	80009	070–9808–00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
					OPTIONAL ACCESSORIES		
	070-9802-00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00

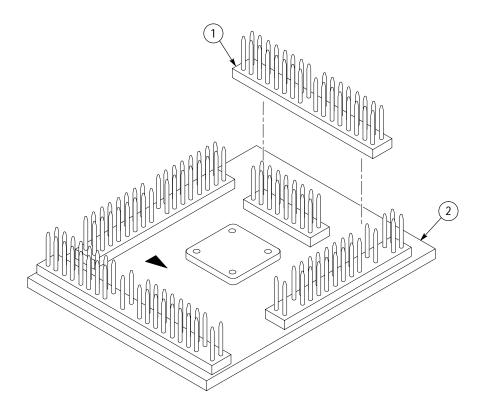


Figure 6–1: 386SX probe adapter exploded view

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